ABSTRACT OF THE INVENTION

An architecture and techniques of the present invention combine multiple queues into a single multientity queue that functions in conjunction with a free queue embodied within the multientity queue. This multientity queue enables a device to significantly decrease overhead of memory clock cycles as data parcels are passed from process to process. The architecture implements a single queue with new pointers in addition to the "old" and "new" pointers associated with conventional queues. These new pointers represent processes or entities and can be referred to as first entity pointer, second entity pointer, third entity pointer and so on.

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